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Memory and Storage solutions for today's world

Accelerated Memory Production, Inc.

COMPACT FLASH (CLASS 5C-SLC)

DESCRIPTION

AMP Inc's storage devices are high capacity, solid-state, non-volatile Flash memory products, which comply with PC Card ATA and True IDE Mode industry standards.

AMP Inc's storage devices are compatible with virtually all of today's computing and communications systems. All AMP Inc's storage products support 3.3V and 5V operation, and 8, 16 and 32-bit technology. Most AMP Inc's storage products can be interchanged between systems, providing the broadest compatibility across platforms.

Flash data storage outperforms all other memory technologies for ruggedness, reliability, capacity, smaller size and low power consumption. The AMP Inc's COMFLASH Card's matchbook size and half-ounce weight make it the world's smallest removable data storage system. The amp inc's COMFLASH Card is ideal for a range of current and next-generation, small-form-factor consumer applications such as digital cameras, cellular phones, PDAs, personal communicators, pagers and audio recorders.

FEATURES

- Easy Installation
- High Performance – up to 40 MB/sec host to buffer
- ATA/IDE Interface – simple Plug and Play PC solution
- Extremely rugged and reliable
- Low-power consumption
- Increased battery life over hard disk use
- Built in "on the fly" ECC and wear leveling
- Support for CIS implemented with 256 bytes of attribute memory
- Available in Industrial Temperature
- Support- UDMA (up to UDMA-6), PCMCIA and IDE
- S.M.A.R.T Capable
- Compact Flash™ Specification version 4.1 Compliant
- RoHS Compliant (Lead-Free)

AMP Part Number	Capacity
AMPCF129M1S-vuxSNyC(I)-5C	128MB
AMPCF257M1S-vuxSNyC(I)-5C	256MB
AMPCF513M1S-vuxSNyC(I)-5C	512MB
AMPCF01DG1S-vuxSNyC(I)-5C	1GB
AMPCF02DG1S-vuxSNyC(I)-5C	2GB
AMPCF04DG1S-vuxSNyC(I)-5C	4GB
AMPCF08DG1S-vuxSNyC(I)-5C	8GB
AMPCF16DG1S-vuxSNyC(I)-5C	16GB
AMPCF32DG1S-vuxSNyC(I)-5C	32GB
AMPCF64DG1S-vuxSNyC(I)-5C	64GB

V = Emulation Mode.
(2 = mixed; 4 = removable; 6 = fixed)
U = Operating Speed
(0 = PIO; 7 = UDMA IDE; 8 = UDMA PCMCIA/IDE)
X = Format option
(F = Formatted; W = RAW)
N = RoHS Compliant (Lead Free)
Y = Component density
I = Industrial Temp.

Product Specification

Operation description

1. Operating Voltage:	Vcc Power	3.3V ±10%;
		5V±10%;
2. Typical Power Consumptions:	3.3V	Read Mode: 20 mA (Max)
		Write Mode: 35 mA (Max)
		Idle Mode: <<0.3mA
	5V	Read Mode: 40 mA (Max)
		Write Mode: 60 mA (Max)
		Standby Mode: <<1mA
3. Environment conditions	Operating Temperature	0°C to +70°C (Standard), -40°C to +85°C (Industrial)
	Storage Temperature	-20°C to +85°C
	Relative Humidity	5% ~ 95% (Max.)
	Shock	2000-G
	Vibration	15-G
4. System Compatibility	0/S support DOS, Windows 98/ME/NT/2000/XP	

Physical Description

1.Weight and Measures (unit: m)	Type I (128MB- 64GB)	Weight: 15 g	L x W x H 36.4 x 42.8 x 3.3(mm)
		Pin-Pitch: 1.27 mm	
2. Storage Capacities	Capacity		128MB-64GB
3. Performance	Data Transfer Rates		Read: up to 35MB/s
			Write: up to 35MB/s
			Sustain Write 18MB/sec
	Data Access Time		1.2 ms
4. Reliability	MTBF		4,000,000 hours*
	Error Correction		Up to 24 random bits in 1024 bytes Correction per second read
	ECC		High reliability based on Internal ECC function
	Endurance		2,000,000 Write/Erase cycles*

Pin Assignment

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
No.	Pin Name	I/O	No.	Pin Name	I/O	No.	Pin Name	I/O
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	#CE1	I	7	#CE1	I	7	#CE1	I
8	A10	I	8	A10	I	8	A10	I
9	#0E	I	9	#OE	I	9	#ATA SEL	I
10	A09	I	10	A09	I	10	A09	I
11	A08	I	11	A08	I	11	A08	I
12	A07	I	12	A07	I	12	A07	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06	I
15	A05	I	15	A05	I	15	A05	I
16	A04	I	16	A04	I	16	A04	I
17	A03	I	17	A03	I	17	A03	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	#I0IS16	O	24	#I0CS16	O
25	#CD2	O	25	#CD2	O	25	#CD2	O
26	#CD1	O	26	#CD1	O	26	#CD1	O
27	D11	I/O	27	D11	I/O	27	D11	I/O
28	D12	I/O	28	D12	I/O	28	D12	I/O
29	D13	I/O	29	D13	I/O	29	D13	I/O
30	D14	I/O	30	D14	I/O	30	D14	I/O
31	D15	I/O	31	D15	I/O	31	D15	I/O
32	#CE2	I	32	#CE2	I	32	#CE2	I
33	#VS1	O	33	#VS1	O	33	#VS1	O
34	#IORD	I	34	#IORD	I	34	#IORD	I
35	#IOWR	I	35	#IOWR	I	35	#IOWR	I
36	#WE	I	36	#WE	I	36	#WE	I
37	RDY/BSY	O	37	IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	#CSEL	I	39	#CSEL	I	39	#CSEL	I
40	#VS2	O	40	#VS2	O	40	#VS2	O
41	RESET	I	41	RESET	I	41	#RESET	I
42	#WAIT	O	42	#WAIT	O	42	IORDY	O
43	#INPACK	O	43	#INPACK	O	43	#INPACK	O
44	#REG	I	44	#REG	I	44	#REG	I
45	BVD2	I/O	45	#SPKR	I/O	45	#DASP	I/O
46	BVD1	I/O	46	#STSCHG	I/O	46	#PDIAG	I/O
47	D08	I/O	47	D08	I/O	47	D08	I/O
48	D09	I/O	48	D09	I/O	48	D09	I/O
49	D10	I/O	49	D10	I/O	49	D10	I/O
50	GND	I/O	50	GND	I/O	50	GND	I/O

Signal Description

Signal Name	I/O	Pin	Description
A0-A10 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17 18,19,20	These address lines along with the #REG signal are used to select the I/O port address registers within the card, the memory mapped port address registers within the Card, a byte in the card's information structure and its configuration control and status registers.
A0-A10 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A0-A10 (True IDE Mode)			In True IDE Mode only A0-A2 are used to select the one of eight registers in the ATA Task File, the others address lines should be grounded.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as the BVD1 signal since a battery is not used with this card.
#STSCHG (PC Card I/O Mode)			This signal is asserted low to alert the host to changes in the RDY/#BSY and Write Protect states, while the I/O interface is configured. The Card Configure and Status Register will control it.
#PDIAG (True IDE Mode)			In the True IDE Mode, this I/O is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is always driven to a high state in Memory Mode since a battery is not required for this card.
#SPKR (PC Card I/O Mode)			This signal is always driven to a high state in I/O Mode since this card does not support the audio function.
#DASP (True IDE Mode)			In the True IDE Mode, this I/O is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
#CD1, #CD2 (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O	25, 26	These Card Detect pins are connected to ground on this card and used by the host to determine that the card is fully inserted into the socket.
#CE1, #CE2 (PC Card Memory Mode) (PC Card I/O Mode)	I	7,32	These signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. #CE2 always accesses the odd byte of the word. #CE1 accesses the even byte or the odd byte of the word depending on A0 and #CE2.
#CE1, #CE2 (True IDE Mode)			In the True IDE Mode, #CE1 is the chip select for the Task File Registers while #CE2 is used to select the Alternate Status and the Device Control Register.
#CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
#CSEL (PC Card I/O Mode)			This signal is not used of this mode.
#CSEL (True IDE Mode)			This internally pulled up signal is used to configure this card as a Master or a Slave. When this pin is grounded, this card is Master. When this pin is open, this card is Slave
D0-D15 (PC Card Memory Mode) (PC Card I/O Mode)	I/O	2,3,4,5 6,21,22,23, 27,28,29, 30,31,47,4 849	These lines carry the Data, Commands and Status between the host and controller. D00 is the LSB of the even byte of the word. D08 is the LSB of the odd byte of the word.
D0-D15 (True IDE Mode)			In True IDE Mode, all Task File operations occur in the byte mode on the low order D00-D07 while all data transfers are 16 bits using D00-D15
GND (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)		1,50	Ground.

#INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
#INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted when the card is selected and responds to an I/O read cycle at the address on the address bus.
#INPACK (True IDE Mode)			In the True IDE mode, this signal is not used.
#IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
#IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the card when the card is configured to used the I/O interface.
#IORD (True IDE Mode)			In the True IDE mode, the signal is the same as the I/O Mode.
#IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode
#IOWR (PC Card I/O Mode)			The I/O Write strobe is used to clock I/O data on the Data bus into the card controller registers when the card is configured to use the I/O interface.
#IOWR (True IDE Mode)			In the True IDE Mode, this signal is the same as the I/O mode.
#OE (PC Card Memory Mode)	I	9	This is an Output Enable Strobe generated by the host interface. It is used to read data from the card in Memory Mode and to read CIS and configuration registers.
#OE (PC Card I/O Mode)			In I/O Mode, this signal is used to read the CIS and configuration registers.
#ATA SEL (True IDE Mode)			To enable True IDE Mode, this signal should be grounded.
RDY/#BSY (PC Card Memory Mode)	O	37	In the Memory Mode, this signal is set high when card is ready to accept a new data transfer operation and held low when the card is busy.
#IREQ (PC Card I/O Mode)			I/O Operation. After the card has been configured for I/O Mode, this signal is used as Interrupt Request.
INTRQ (True IDE Mode)			In the True IDE Mode, this signal is the active high Interrupt Request to the host.
#REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycle to distinguish between Common Memory and Attribute Memory accesses. High for Common Memory and Low for Attribute Memory.
#REG (PC Card I/O Mode)			This signal must be low during I/O Cycles when the I/O address is on the Bus.
#REG (True IDE Mode)			In the True IDE Mode, this signal is not used and should be connected to VCC by the host.

RESET (PC Card Memory Mode)	I	41	When the signal is high, the signal Resets the card.
RESET (PC Card I/O Mode)			When the signal is high, the signal Resets the card.
#RESET (True IDE Mode)			In the True IDE Mode, the signal is the active low hardware reset from the host.
VCC (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)		13, 38	5V, 3.3V
#VS1, #VS2 (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O	33, 40	Voltage Sense Signals.
#WAIT (PC Card Memory Mode) (PC Card I/O Mode)	O	42	This signal is driven low by the card to notify the host to delay completion of the memory of I/O cycle that is in progress.
IORDY (True IDE Mode)			In the True IDE Mode, this signal may be used as IORDY.
#WE (PC Card Memory Mode)	I	36	This signal is driven by the host and used for generating memory write cycle to the registers of the card when the card is configured in the Memory Mode.
#WE (PC Card I/O Mode)			In I/O mode, this signal is used for writing the configuration registers.
#WE (True IDE Mode)			In the True IDE Mode, this signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	Memory Mode, the card doesn't have a write protect switch. This signal is held low.
#IOIS16 (PC Card I/O Mode)			I/O Mode, A low signal indicates that a 16 bits or odd byte only operation can be performed by the addressed port.
#IOIS16 (True IDE Mode)			In the True IDE Mode, this signal is asserted low when this device is expecting a word data transfer cycle.

Overlapping I/O Mapping Addressing

Overlapping I/O Mapping (Primary, Secondary) Addressing

#REG	A10	A4-A9		A3	A2	A1	A0	#IORD="0"	#IOWR="0"
		Primary	Secondary						
0	X	1FH	17H	0	0	0	0	Even read Data	Even write Data
0	X	1FH	17H	0	0	0	1	Error	Feature
0	X	1FH	17H	0	0	1	0	Sector Count	Sector Count
0	X	1FH	17H	0	0	1	1	Sector Number	Sector Number
0	X	1FH	17H	0	1	0	0	Cylinder Low	Cylinder Low
0	X	1FH	17H	0	1	0	0	Cylinder High	Cylinder High
0	X	1FH	17H	0	1	1	0	Drive/Head	Drive/Head
0	X	1FH	17H	0	1	1	1	Status	Command
0	X	3FH	37H	1	1	1	0	Alternate Status	Device Control
0	X	3FH	37H	1	1	1	1	Drive Address	Reserved

True IDE Mode

True IDE Mode

#CS0	#CS1	DA2	DA1	DA0	#IORD="0"	#IOWR="0"
1	1	X	X	X	Hi-Z	Not Used
1	0	0	X	X	Hi-Z	Not Used
1	0	1	0	X	Hi-Z	Not Used
0	0	X	X	X	Invalid	Invalid
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command

Card Configuration Registers

The table summarizes the drive four PCMCIA configuration registers. These read/write one-byte registers are located on even-byte attribute-plane addresses to ensure access in 8- and 16-bit system. Available card status information allows arbitration between resources that share interrupts and status of memory-only-card pins 16, 32, 62, and 63.

Register	Add. Off-set[1]	R/W	REG#	CE2#	CE1#	OE#	WE#	D15-8	D7-0
Configuration Option	200h	Read	L	H	L	L	H	Invalid	Option
		Write	L	H	L	H	L	Invalid	Option
Card Configuration And Status	202h	Read	L	H	L	L	H	Invalid	Status
		Write	L	H	L	H	L	Invalid	Config.
Pin Replacement	204h	Read	L	H	L	L	H	Invalid	Pin Status
		Write	L	H	L	H	L	Invalid	Pin Status
Socket and Copy	206h	Read	L	H	L	L	H	Invalid	Socket ID
		Write	L	H	L	H	L	Invalid	Socket ID

Notes
1 the host obtains attribute-memory address offset from the Configuration Tuple tpcc_radr field when it reads the drive CIS.

Configuration Option Register

The host uses the read/write Configuration Option register to configure the drive for drive for one of its four PCMCIA-ATA addressing modes, establish the interrupt signal mode, and issue a soft reset.

7	6	5	4	3	2	1	0
SRST	IRQLv1	Configuration Index					

SRST Resets the card when 1. When 0 (default) after a hardware or software reset or power-on, the card is unconfigured. A configuration occurs when a valid configuration index is written to bits 0-5.

IRQLv1 Selects level mode interrupts when 1, pulse mode interrupts when 0 (default).

Conf IDX The host chooses an option from the card configuration table entry tuples and writes that option Configuration Index number into this field. When zero (default), the memory-only interface is chosen, I/O accesses are disabled.

Configuration & Status Register

The Configuration and Status register contains card condition information.

7	6	5	4	3	2	1	0
Chng	**SigChg**	**Iois8**	**0**	**Audio**	**PwrDn**	**Intr**	**0**

Chng The Change bit indicates that a Pin Replacement register bit was changed.

SigChg The host sets/resets the Signal Changed bit to enable/disable a state-change signal from the status register. When set and the drive is configured for I/O, Chng controls pin 63 and is called the Changed Status signal. This bit should be 0 (BVD1/STSCHG# held high when configured for I/O) if no state change signal is desired.

IOis8 Must be set if the host can only perform 8-bit I/O accesses.
Audio Audio is not supported
PwrDN Setting PwrDn places the drive in sleep mode. Host-initiated ATA task-file-register commands can also invoke low-power modes.
Intr This bit represents the interrupt request internal state. Its value is available whether or not interrupts are configured. It remains true until the initiating-interrupt request is serviced.

Pin Replacement Register

The Pin Replacement register provides card status information that is otherwise provided on memory-only interface pin 16, 33, 62, and 63. When written, bits 0-3 are masks for setting corresponding bits 4-7.

7	6	5	4	3	2	1	0
CBvd	**CBvd**	**Crdy/bsy#**	**CWP**	**RBvd**	**RBvd**	**Rrdy/bsy#**	**RWP**

CBvd1, 2 Set when written, otherwise zero.
Crdy/bsy# Set when Rrdy/bsy# changes state or when written by the host.
CWP Zero unless set by the host.
RBvd1, 2 Set unless cleared by the host.
Rrdy/bsy# Internal ready/busy# state when I/O mode uses RDY/BSY# pin for interrupt.
RWP Zero, since the flash drive has no write protect switch, unless set by the host.

Socket and Copy Register

The Socket and Copy register allows the drive to distinguish between similar drives at the same address. The flash drive does not support this feature.

7	6	5	4	3	2	1	0
0	**Copy Number**			**Socket Number**			

Copy # The twin-card option is not supported

Socket# The socket number is ignored.

Task File Registers

Data is transferred between the host and the card and the transfer controlled via the task file registers. The task file registers refer t the following series of registers.

1) Data register
2) Error register
3) Feature register
4) Sector count register
5) Sector number register
6) Cylinder low register
7) Cylinder High register
8) Drive head register
9) Status register
10) Alternate status register
11) Command register
12) Device control register
13) Drive address register

These registers are divided into five mapping modes (1) memory mapping, (2) primary I/O mapping, (3) secondary I/O mapping, (4) contiguous I/O mapping and (5) True-IDE mode I/O mapping, according to the address spaces to which these registers are assigned. The mapping mode is selected after the host writes a value in INDEX of the configuration optional register. Each mapping mode is explained below.

In the memory-mapping mode, the task file registers are assigned to the common memory area (see figure 3.3 below). As described in CIS (TPCE_FA and TPCE_MS of the configuration entry tuple), the memory window size is set at 2 Kbytes and the card base address at "0H". This window can be mapped to any address in the memory address space of the host. The position of the task file registers is determined by the offset address from the card base address. The 1-Kybte-memory window from offset "400H" to "7FFH" is secured for the host to access the data register during block transfer from memory to memory. Since this 1-Kbyte-memory window accesses F1F0, data cannot be accessed randomly.

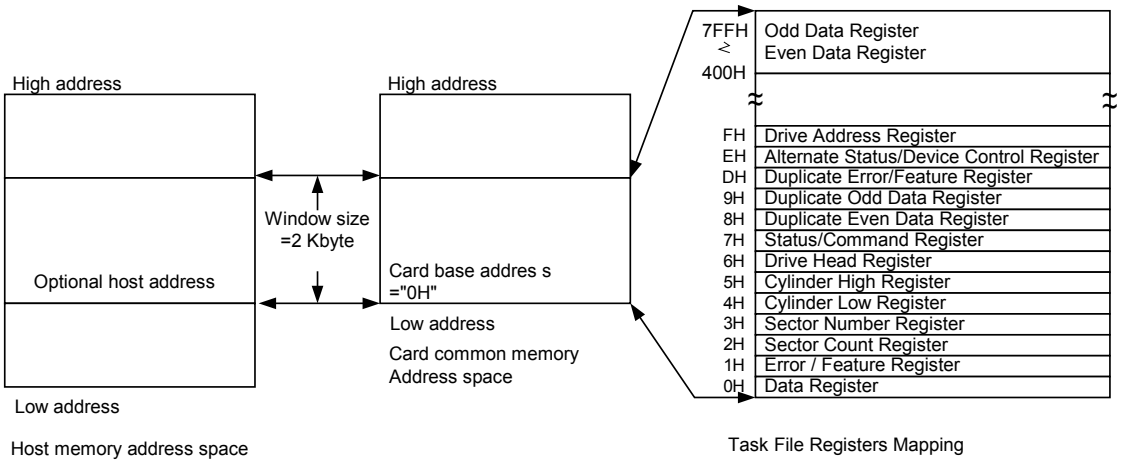

Figure 3.3 Memory Mapping Mode

In the primary or secondary I/O mapping mode, the register functions as the I/O card to be accessed via "1F0H" to "1F7H" and "3F6H" to "3F7H" (primary) or "170H" to "177H" and "376H" to "377H" (secondary) in the standard I/O address space. Address signals of A9 to A0 are used for access and A10 neglected.

In the contiguous I/O mapping mode, only four address signals of A3 to A0 in the I/O address space are decoded. Thanks to this function, those other than A3 to A0 can be accessed via any address although host operation is required.

Table 3.3 shows task file registers mapping in the I/O card mode. The contiguous I/O mapping mode has the data and error/feature registers as well as the duplicate even data, duplicate odd data and duplicate error/feature registers. The data register can be accessed as 16-bit data combining 8-bit data indicated by an even address and 8-bit data indicated by an odd address. Since the data register overlaps the error/feature register when handled as 16-bit data, registers duplicating them are equipped.

Table 3.3 Memory and I/O Modes Decoding

Primary I/O Map A9 to A0	Secondary I/O Map A9 to A0	Contiguous Map A3 to A0	Task file register
1F0H	170H	0H	Data register
1F1H	171H	1H	Error/feature register
1F2H	172H	2H	Sector count register
1F3H	173H	3H	Sector number register
1F4H	174H	4H	Cylinder low register
1F5H	175H	5H	Cylinder high register
1F6H	176H	6H	Drive head register
1F7H	177H	7H	Status/command register
-	-	8H	Duplicate even data register
-	-	9H	Duplicate odd data register
-	-	DH	Duplicate error/feature register
3F6H	376H	EH	Alternate status/device control register
3F7H	377H	FH	Drive address register

In the True-IDE mode I/O mapping mode, only three address signals of A2 to A0 in the I/O address space are decoded as shown in table 3.4, and the –CE2 signal is used to select the alternate status/ device control or drive address register and the –CE1 to select other task file registers.

Table 3.4 True-IDE Mode Decoding

-CE2	-CE1	True-IDE Mode I/O map A2 to A0	Task file register
1	0	0H	Data register
1	0	1H	Error/feature register
1	0	2H	Sector count register
1	0	3H	Sector number register
1	0	4H	Cylinder low register
1	0	5H	Cylinder high register
1	0	6H	Drive head register
1	0	7H	Status/command register
0	1	6H	Alternate status/device control register
0	1	7H	Drive address register

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Function	ADDR	R/W	REG#	CE2#	CE1#	0E#	WE#	IORD#	IOWR#	D15-8	D7-0
No Operation	X[1]		X	H	H	X	X	X	X	High-Z	High-Z
Data (see note 3)	000	Read	H	L	L	L	H	H	H	Data High	Data Low
			H	H	L	L	H	H	H	Invalid	Data
		Write	H	L	L	H	L	H	H	Data High	Data Low
			H	H	L	H	L	H	H	Invalid	Data
Error	001	Read	H	H	L	L	H	H	H	Invalid	Error
			H	L	H	L	H	H	H	Error	Invalid
Set Feature		Write	H	H	L	H	L	H	H	Invalid	Feature
			H	L	H	H	L	H	H	Feature	Invalid
Sector Count	002	Read	H	X	L	L	H	H	H	Invalid	Sect. Cnt.
		Write	H	X	L	H	L	H	H	Invalid	Sect. Cnt.
Sector Number	003	Read	H	H	L	L	H	H	H	Invalid	Sect. No.
			H	L	H	L	H	H	H	Sect. No.	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Sect. No.
			H	L	H	H	L	H	H	Sect. No.	Invalid
Cylinder Low	004	Read	H	X	L	L	H	H	H	Invalid	Cyl. Low
		Write	H	X	L	H	L	H	H	Invalid	Cyl. Low
Cylinder High	005	Read	H	H	L	L	H	H	H	Invalid	Cyl. High
			H	L	H	L	H	H	H	Cyl. High	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Cyl. High
			H	L	H	H	L	H	H	Cyl. High	Invalid
Drive/Head	006	Read	H	X	L	L	H	H	H	Invalid	Drv/Hd
		Write	H	X	L	H	L	H	H	Invalid	Drv/Hd
Status	007	Read	H	L	L	L	H	H	H	Invalid	Status
			H	H	H	L	H	H	H	Status	Invalid
Command		Write	H	L	L	H	L	H	H	Invalid	Command
			H	H	H	H	L	H	H	Command	Invalid
Data (duplicate) (see note 3)	008	Read	H	L	L	L	H	H	H	Data High	Data Low
			H	H	L	L	H	H	H	Invalid	Data
		Write	H	L	L	H	L	H	H	Data High	Data Low
			H	H	L	H	L	H	H	Invalid	Data
	009	Read	H	H	L	L	H	H	H	Invalid	Data High
			H	L	H	L	H	H	H	Data High	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Data High
			H	L	H	H	L	H	H	Data High	Invalid
Invalid	00A – 00C		H	X	X	X	H	X	X	Invalid	Invalid
Error (duplicate)	00D	Read	H	H	L	L	H	H	H	Invalid	Error
			H	L	H	L	H	H	H	Error	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Feature
			H	L	H	H	L	H	H	Feature	Invalid
Alternate Status	00E	Read	H	X	L	L	H	H	H	Invalid	Alt. Status
Drive Control		Write	H	X	L	H	L	H	H	Invalid	Control
Drive Address	00F	Read	H	H	L	L	H	H	H	Invalid	Drv. Add.
			H	L	H	L	H	H	H	Drv. Add	Invalid
		Write	H	H	L	H	L	H	H	Invalid	Not Used
			H	L	H	H	L	H	H	Not Used	Invalid
Data (duplicate) (see note 3)	400-7FF	Read	H	L	L	L	H	H	H	Data High	Data Low
		Write	H	L	L	H	L	H	H	Data High	Data Low

1 X = don't care

2 The host must decode addresses All and above to provide card enables CE1# and CE2# that place the drive on a 2-K byte Boundary
The drive decodes A0-10

3 In independent memory mode, each byte access to 000, 008, or even addresses 400-7FE presents a new data buffer words on D0-15 Byte access to 009 or odd addresses 401-7FF present high byte buffer data on D0-7 or D8-15 depending on CDE1# and CE2#

I/O Mode Decoding

Starting with PCMCIA's PC Card standard 2.0, system I/O space can be used to access PC cards. The flash drive provides three I/O addressing modes:

- Independent I/O allows the drive to be mapped at any 16-byte I/O boundary. The host must decode I/O addresses A4 and above to provide card-enables CE1# and CE2#. The drive decodes addresses A0-3.
- Primary drive address at system ATA I/O address 1 F0h-1F7h and 3F6h-3F7. The host must decode I/O addresses A10 and above to provide card-enables CE1# and CE2#. The drive decodes addresses A0-9.
- Secondary drive address at system ATA I/O address 170h-177h and 376h-377. The host must decode addresses A10 and above to provide card-enables CE1# and CE2#. The drive decodes addresses A0-9. Independent I/O mode is the most flexible because it allows host to place the drive at any available 16-byte I/O address boundary. A system can use multiple flash drives, limited only by available 16-contiguous-byte I/O spaces.
- Primary and secondary drive addressing modes allow hosts to use the AT-standard's reserved disk drive I/O addressee. This provides PC system designers with the simplest way to accommodate ATA-protocol devices. Once the PCMCIA socket adapter is configured for the primary or secondary drive address ranges, a PC can take advantage of the BIOS's standard disk access routines.
- Additionally, since the PC's host adapter must decode addresses A10 and above within its 64-Kbyte I/O space, up to PCMCIA-ATA drivers can be placed at 4-kbyte boundaries. For example, drives can be placed at primary-type I/O addresses 01F0h, 11F0h, and 21F0h, … F1F0h. Drives can also be placed at secondary-type I/O addresses 0170h, 1170h, 2170h, F170h

The following truth table shows PCMCIA-ATA I/O address modes.

PCMCIA-ATA MODE-Independent I/O address = xx0-xxF[2]

Function	ADDR	R/W	REG#	CE2#	CE1#	0E#	WE#	IORD#	IOWR#	D15-8	D7-0
No Operation	X[1]		X	H	H	X	X	X	X	High-Z	High-Z
Data	0	Read	L	H	L	H	H	L	H	Invalid	Data Low
			L	L	L	H	H	L	H	Data High	Data Low
		Write	L	H	L	H	H	H	L	X	Data Low
			L	L	L	H	H	H	L	Data High	Data Low
Error	1	Read	L	H	L	H	H	L	H	Invalid	Error
			L	L	H	H	H	L	H	Error	Invalid
Set Feature		Write	L	H	L	H	H	H	L	X	Feature
			L	L	H	H	H	H	L	Feature	X
Sector Count	2	Read	L	H	L	H	H	L	H	Invalid	Sect. Cnt.
				L	L	H	H	L	H	Sect. Cnt.	Sect. Cnt.
		Write	L	H	L	H	H	H	L	X	Sect. Cnt.
				L	L	H	H	H	L	Sect. No.	Sect. Cnt.
Sector Number	3	Read	L	H	L	H	H	L	H	Invalid	Sect. No.
			L	L	H	H	H	L	H	Sect. No.	Invalid
		Write	L	H	L	H	H	H	L	X	Sect. No.
			L	L	H	H	H	H	L	Sect. No.	X
Cylinder Low	4	Read	L	H	L	H	H	L	H	Invalid	Cyl. Low
				L	L	H	H	L	H	Cyl. High	Cyl. Low
		Write	L	X	L	H	H	H	L	X	Cyl. Low
				X	L	H	H	H	L	Cyl. High	Cyl. Low
Cylinder High	5	Read	L	H	L	H	H	L	H	Invalid	Cyl. High
			L	L	H	H	H	L	H	Cyl. High	Invalid
		Write	L	H	L	H	H	H	L	X	Cyl. High
			L	L	H	H	H	H	L	Cyl. High	X
Drive/Head	6	Read	L	H	L	H	H	L	H	Invalid	Drv/Hd
				L	L	H	H	L	H	Status	Drv/Hd
		Write	L	H	L	H	H	H	L	X	Drv/Hd
				L	L	H	H	H	L	Command	Drv/Hd
Status	7	Read	L	H	L	H	H	L	H	Invalid	Status
			L	L	H	H	H	L	H	Status	Invalid
Command		Write	L	H	L	H	H	H	L	X	Command
			L	L	H	H	H	H	L	Command	X
Data (duplicate)	8	Read	L	H	L	H	H	L	H	Invalid	Data Low
			L	L	L	H	H	L	H	Data High	Data Low
		Write	L	H	L	H	H	H	L	X	Data Low
				L	L	H	H	H	L	Data High	Data Low
	9	Read	L	H	L	H	H	L	H	Invalid	Data High
			L	L	H	H	H	L	H	Data High	Invalid
		Write	L	H	L	H	H	H	L	X	Data High
			L	L	H	H	H	H	L	Data High	X
Invalid	A – C		L	X	X	X	X	X	X	Invalid	Invalid
Error (duplicate)	D	Read	L	H	L	H	H	L	H	Invalid	Error
			L	L	H	H	H	L	H	Error	Invalid
		Write	L	H	L	H	H	H	L	X	Feature
			L	L	H	H	H	H	L	Feature	X
Alternate Status	E	Read	L	H	L	H	H	L	H	Invalid	Alt Status
			L	L	L	H	H	L	H	Drv. Add	Alt Status
Drive Control		Write	L	H	L	H	H	H	L	X	Control
			L	L	L	H	H	H	L	Not Used	Control
Drive Address	F	Read	L	H	L	H	H	L	H	Invalid	Drv. Add
			L	L	H	H	H	L	H	Driv. Add	Invalid
		Write	L	H	L	H	H	H	L	X	Not Used
			L	L	H	H	H	H	L	Not used	X

PCMCIA-ATA MODE-Primary address = 1F0-1F7, 3F6-3F7; Secondary address = 170-177, 376-377[3]

Function	ADDR	R/W	REG#	CE2#	CE1#	0E#	WE#	IORD#	IOWR#	D15-8	D7-0
No Operation	X[1]		X	H	H	X	X	X	X	High-Z	High-Z
Data	0	Read	L	H	L	H	H	L	H	Invalid	Data Low
			L	L	L	H	H	L	H	Data High	Data Low
		Write	L	H	L	H	H	H	L	X	Data Low
			L	L	L	H	H	H	L	Data High	Data Low
Error	1	Read	L	H	L	H	H	L	H	Invalid	Error
			L	L	H	H	H	L	H	Error	Invalid
Set Feature		Write	L	H	L	H	H	H	L	X	Feature
			L	L	H	H	H	H	L	Feature	X
Sector Count	2	Read	L	H	L	H	H	L	H	Invalid	Sect. Cnt.
			L	L	L	H	H	L	H	Sect. Cnt.	Sect. Cnt.
		Write	L	H	L	H	H	H	L	X	Sect. Cnt.
			L	L	L	H	H	H	L	Sect. No.	Sect. Cnt.
Sector Number	3	Read	L	H	L	H	H	L	H	Invalid	Sect. No.
			L	L	H	H	H	L	H	Sect. No.	Invalid
		Write	L	H	L	H	H	H	L	X	Sect. No.
			L	L	H	H	H	H	L	Sect. No.	X
Cylinder Low	4	Read	L	H	L	H	H	L	H	Invalid	Cyl. Low
			L	L	L	H	H	L	H	Cyl. High	Cyl. Low
		Write	L	X	L	H	H	H	L	X	Cyl. Low
			L	X	L	H	H	H	L	Cyl. High	Cyl. Low
Cylinder High	5	Read	L	H	L	H	H	L	H	Invalid	Cyl. High
			L	L	H	H	H	L	H	Cyl. High	Invalid
		Write	L	H	L	H	H	H	L	X	Cyl. High
			L	L	H	H	H	H	L	Cyl. High	X
Drive/Head	6	Read	L	H	L	H	H	L	H	Invalid	Drv/Hd
			L	L	L	H	H	L	H	Status	Drv/Hd
		Write	L	H	L	H	H	H	L	X	Drv/Hd
				L	L	H	H	H	L	Command	Drv/Hd
Status	7	Read	L	H	L	H	H	L	H	Invalid	Status
			L	L	H	H	H	L	H	Status	Invalid
Command		Write	L	H	L	H	H	H	L	X	Command
			L	L	H	H	H	H	L	Command	X
Invalid	A – C		L	X	X	X	X	X	X	Invalid	Invalid
Alternate Status	E	Read	L	H	L	H	H	L	H	Invalid	Alt Status
			L	L	L	H	H	L	H	Drv. Add	Alt Status
Drive Control		Write	L	H	L	H	H	H	L	X	Control
			L	L	L	H	H	H	L	Not Used	Control
Drive Address	F	Read	L	H	L	H	H	L	H	Invalid	Drv. Add
			L	L	H	H	H	L	H	Driv. Add	Invalid
		Write	L	H	L	H	H	H	L	X	Not Used
			L	L	H	H	H	H	L	Not used	X

Table 4 PCMCIA Mode Power-On and Reset Timing Parameters

Symbol	Parameter	Min	Max	Units
tsu (Vcc)	CE# setup time from Vcc	20		ms
tsu (RESET)	CE# setup time from reset	20		ms
trec (VCC)	CE# recovery time	0.001		ms
tp	Vcc rise time [10% to 0.9 (Vcc+5%]	0.1	300	ms
tp0	Vcc fall time [0.9 (Vcc-5%) to 10%]	3.0	300	ms
tw (Reset)	Reset pulse width	10		ms
th (Reset)	Reset high from Vcc min	1		ms
ts (Reset)	Reset high-z from Vcc min	0		ms

Note
I tpr and tpf are linear waveforms' during the 10% to 90% (or vice-versa) period Even if the waveform is not a linear waveform, its rise and fall times must meet this specification.

Table 5 Attribute-Mode Timing Parameters

Symbol	IEEE	Parameter	Min	Max	Units
READ					
t1	tAVAVR	Read cycle time	300		ns
t2	tAVQV	Address access time		300	ns
t3	tELQV	Card Enable access time		300	ns
t4	tGLQNZ	Output Enable to data change	5		ns
t5	tGLQV	Output Enable access time		150	ns
t6	tGLWtV	Wait Valid from Output Enable		35	ns
t7	tWtLWtH	Wait pulse width		12	ns
t8	tQVWtH	Data setup for Wait released	0		ns
t9	tAXQX	Data valid after address change	0		ns
t10	tGHEH	Card Enable hold time	20		ns
t11	tEHQZ	Data disable from Card Enable high		100	ns
t12	tGHQZ	Data disable from Output Enable high		100	ns
WRITE					
t0	tAVAVW	Write cycle time	250		ns
t13	tAVWH	Address valid to Write Enable high	180		ns
t14	tELWH	Card Enable to Write Enable high	180		ns
t15	tWLWH	Write Enable pulse width high	150		ns
t16	tDVWH	Data valid to Write Enable high	80		ns
t17	tAVWL	Address, valid to Write Enable low	30		ns
t18	tELWL	Card Enable setup to Write Enable low	0		ns
t19	tWLQZ	Write Enable to previous		100	ns
t20	tWHDX		30		ns
t21	tWHQNZ		5		ns
t22	tWHAX		30		ns

Attribute-Mode Timing

Attribute memory's access time is 300ns at standard Vcc=3.3V/5V ±5% operating voltage.

Figure 6 and Table 14 show detailed timing specifications.

Address, Reg#

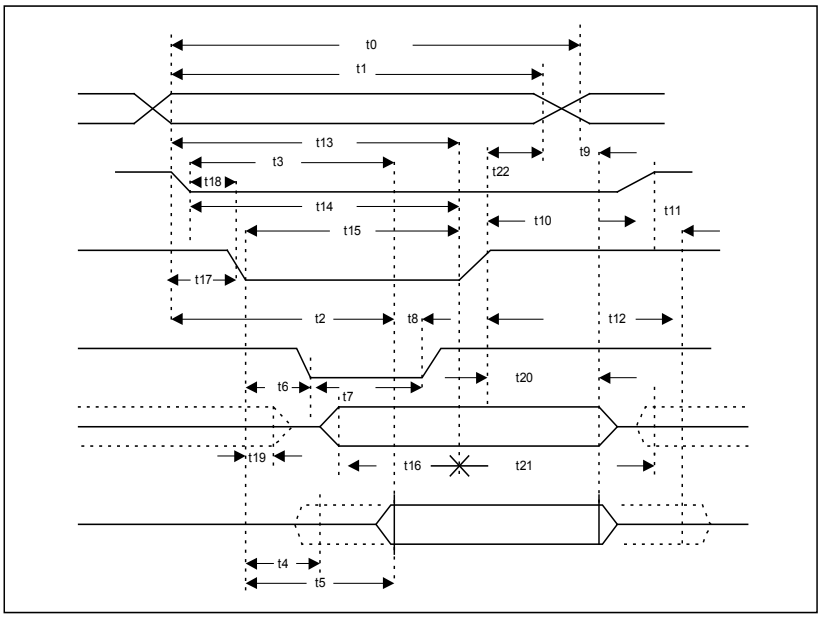
CE1#, CE2#

OE#, WE#

WAIT#

Write Data (D0-15 or D0-7)

Read Data (D0-15 or D0-7)

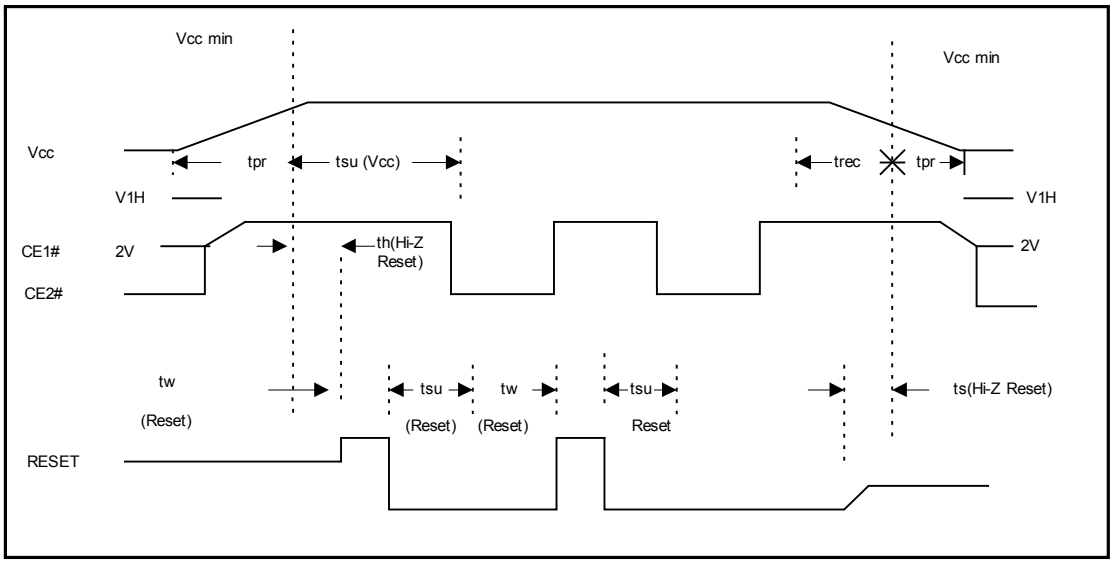


Interface Bus Timing

Several bus timing must be considered when using the flash drive in PCMCIA modes: reset, attribute (or CIS-tuple), common-memory, and I/O timing.

PCMCIA Reset Timing

The flash drive requires some initialization time after a power-on or hardware reset. This time is specified below.

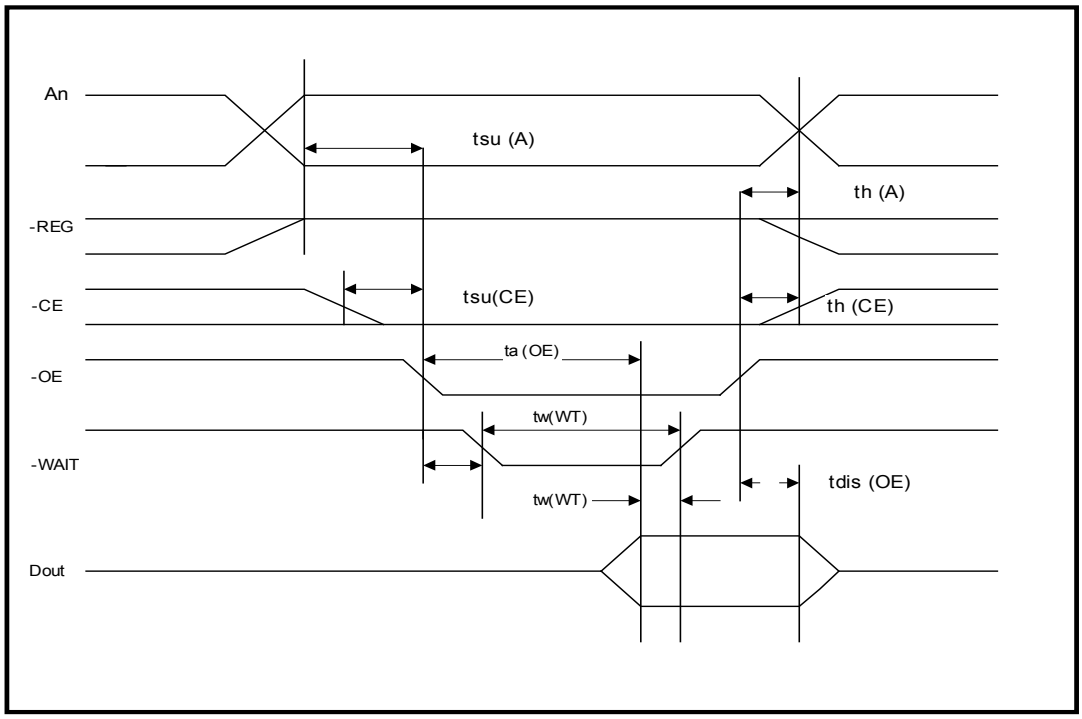


Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(OE)	tAVGL	30	
Address Hold Time	th(A)	tGHAX	30	
CE Setup before OE	tsu(CE)	tELGL	0	
CE Hold following OE	th(CE)	tGHEH	20	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35
Data Setup for Wait Release	tv(WT)	tQVWTH		0
Wait Width Time (Default Speed)	tw(WT)	tWTLWTH		350

Note: The maximum load on-WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds. Dout signifies data prvides by the Compact Flash Memory Card to the system. The-WAIT signal may be ignored if the-OE cycle time is greater than the Wait Width time.

The Max Wait Width time (in the slowest mode) can be determined from the Card Information Structure. [GC]



Common Memory Read Timing Diagram

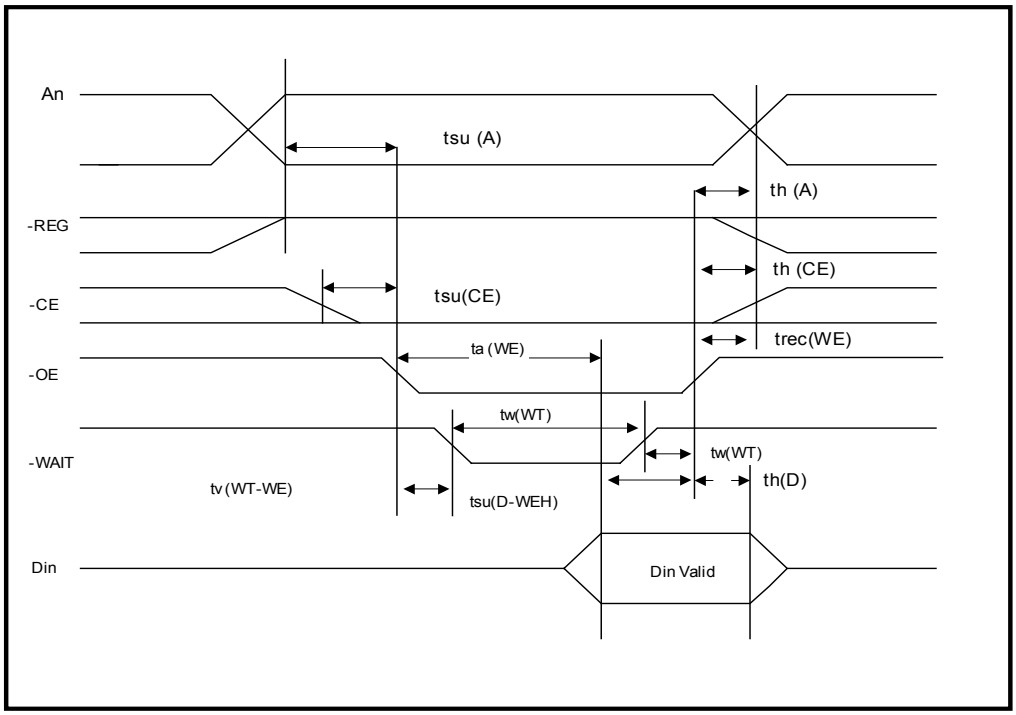
Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before WE	tsu (D-WEH)	tVWH	80	
Data Hold following WE	th (D)	tIWMDX	30	
WE Pulse Width	tw (WE)	tWLWH	150	
Address Setup Time	tsu (A)	tAVWL	30	
CE Setup before WE	tsu (CE)	tELWL	0	
Write Recovery Time	trec (WE)	tWMAX	30	
Address Hold Time	th (A)	tGHAX	20	
CE Hold following WE	th (CE)	tGHEH	20	
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35
WE High from Wait Release	tv (WT)	tWTHWH	0	
Wait Width Time (Default Speed)	tw (WT)	tWTLWTH		350

Note: The maximum load on-WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds. Din signifies data provided by the system to the Compact Flash Memory Card.

The-WAIT signal may be ignored if the-WE cycle to cycle time is greater than the Wait Width time.

The Max Wait Width time (in the slowest mode) can be determined from the Card Information Structure. [GC]



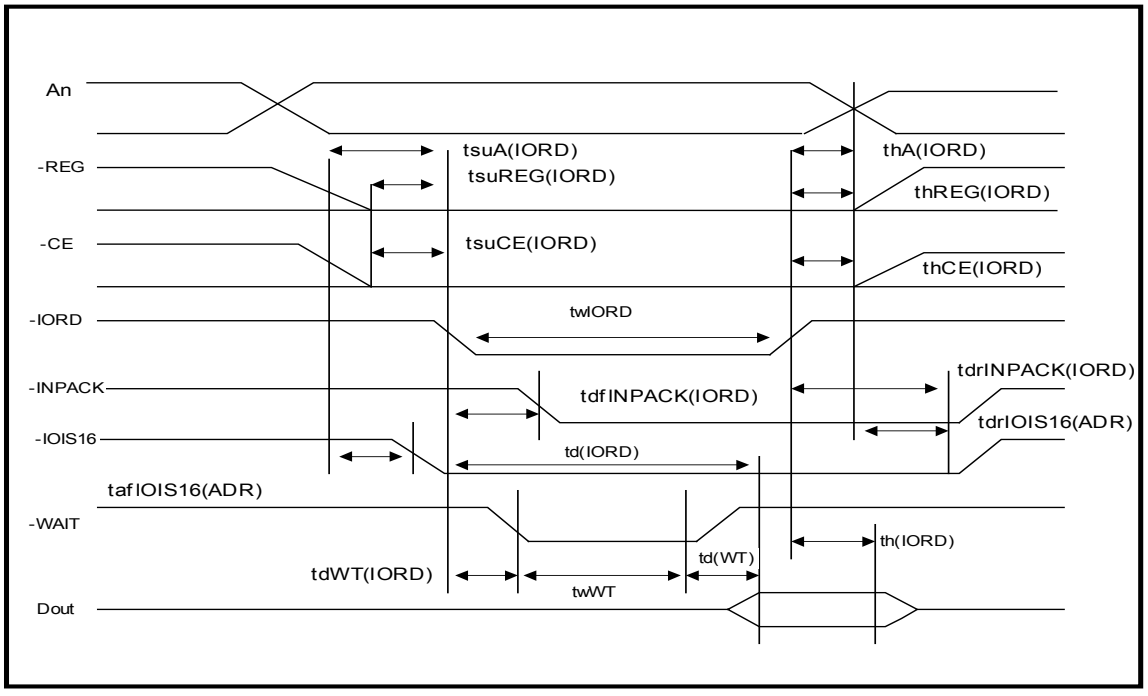
Common Memory Write Timing Diagram

I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	t1GHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfInpack(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrInpack(IORD)	tIGHIAL		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdfIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL		35
Data Delay from Wait Rising	td(WT)	tWTHQV		0
Wait Width Time (Default Speed)	tTd(WT)	tWTLWTH		350

Note: The maximum load on-WAIT, -INPACK and –IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from –WAIT high to –IORD high is 0 nsec, but minimum –IORD width must still be met.

Dout signifies data provides by the compact Flash Memory Card to the system.



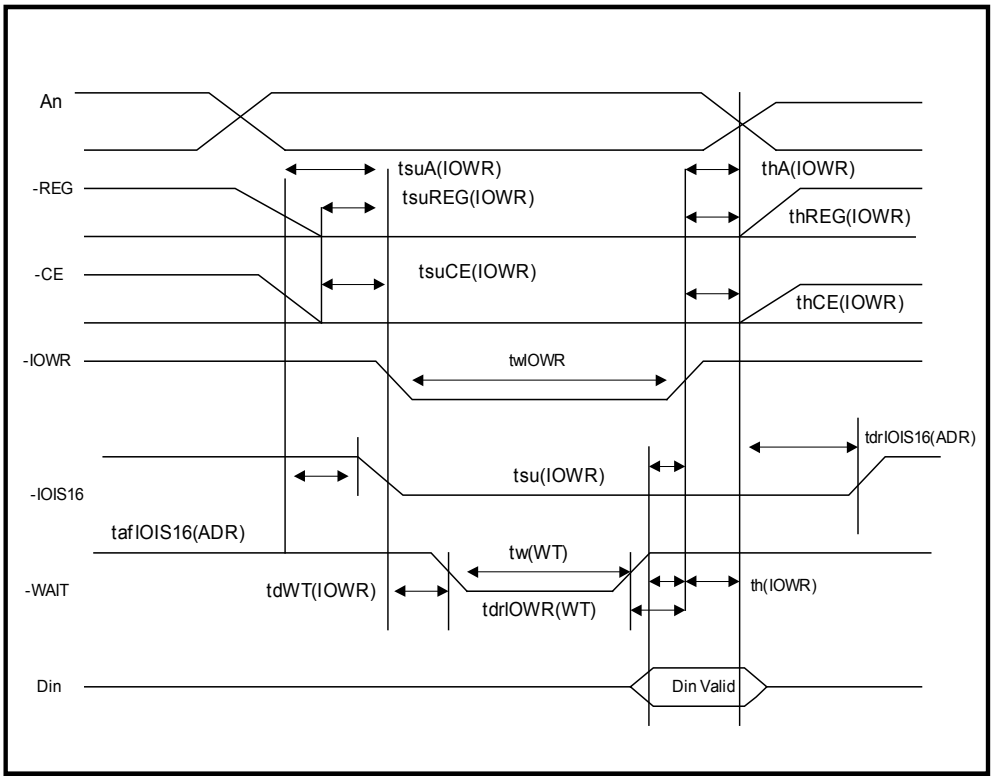
I/O Read Timing Diagram

I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup Before IOWR[GC]	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tlWHDX	30	
IOWR Width Time	twIOWR	tlWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tlWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tlWHEH	20	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG(IOWR)	tlWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADRP	tAVISH		35
Wait Delay Falling from IOWR	tdWT(IOWR)	tlWLWTL		35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	
Wait Width Time (Default Speed) (Set Feature Speed<68mA)	tw(WT	tWTLWTH		350 700

Note: The maximum load on-WAIT, -INPACK and –IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds.

Minimum time from –WAIT high to –IOWR high is 0 nsec, but minimum –IOWR width must still be met. Din signifies data provides by the system to the compact Flash Memory Card.



I/OWrite Timing Diagram

4.3.14 True IDE Mode I/O Input/Output (Read/Write) Timing Specification

The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the –IOWR and the –IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 19: True IDE Mode I/O Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Mode 5 (ns)	Mode 6 (ns)	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to –IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to –IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to –IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	n/a	n/a	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	n/a	n/a	
tC	IORDY assertion to release (max)	5	5	5	5	5	n/a	n/a	

Notes:

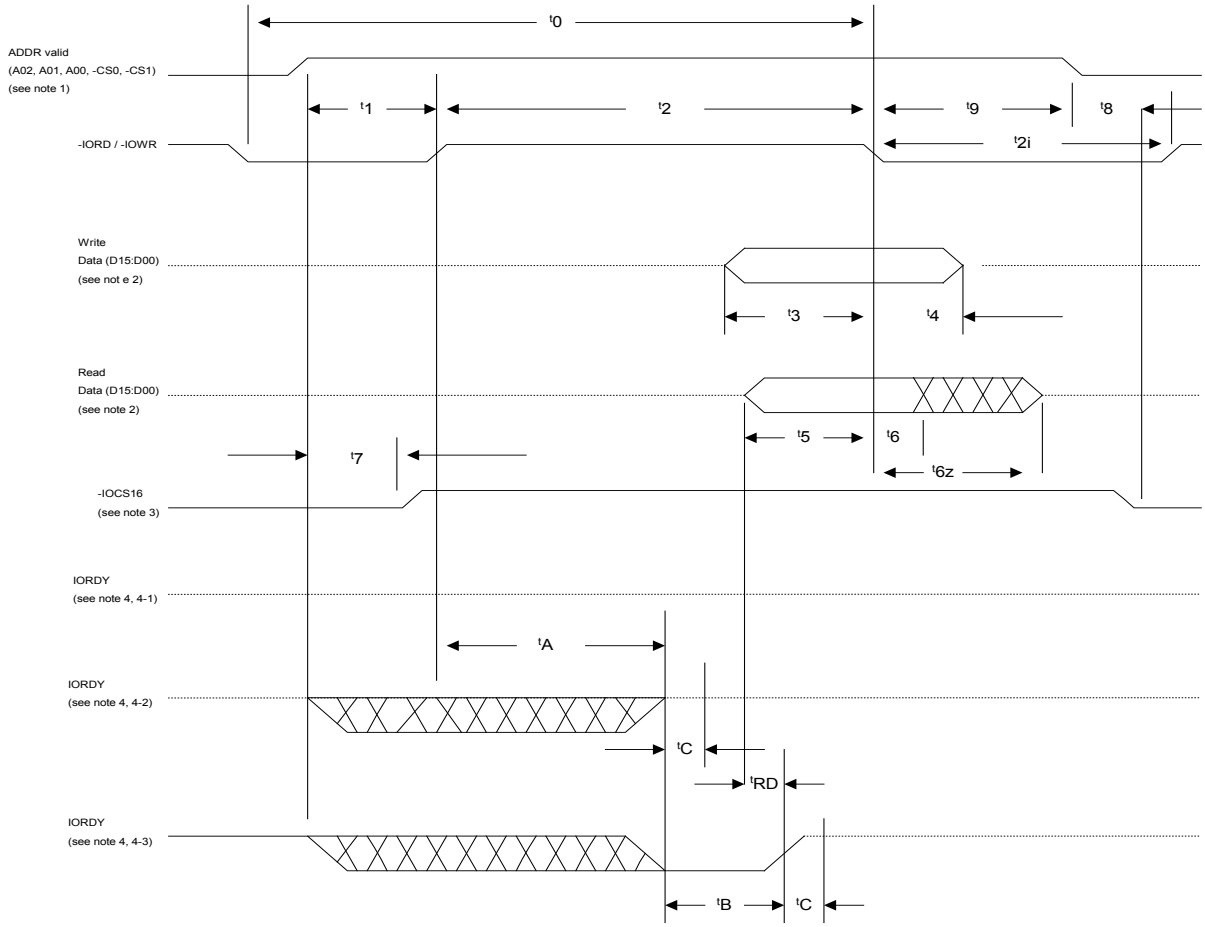
The maximum load on –IOCS16 is 1 LSTTL with a 50 pF total load. All times are in nanoseconds. Minimum time from –IORDY high to –IORD high is 0 nsec, but minimum –IORD width must still be met.

(1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify drive data. A CompactFlash Storage Card implementation shall support any legal host implementation.

(2) This parameter specifies the time from the negation edge of –IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).

(3) The delay from the activation of –IORD or –IOWR until the stat of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORD is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of –IORD or –IOWR, then t5 shall be metand tRD is not applicable. If the CompactFlash Staorage Card is driving IORDY negated at the time tA after the activiation of –IORD or –IOWR, then tRD shall be met and t5 is not applicable.

(4) t7 and t8 appply only to modes 0, 1 and 2. For other modes, this signal is not valid.



Notes:

(1) Device address consists of –CS0, -CS1, and A[02::00]

(2) Data consists of D [15::00] (16-bit) or D [07::00] (8 bit)

(3) –IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of –IORD or IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and –IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

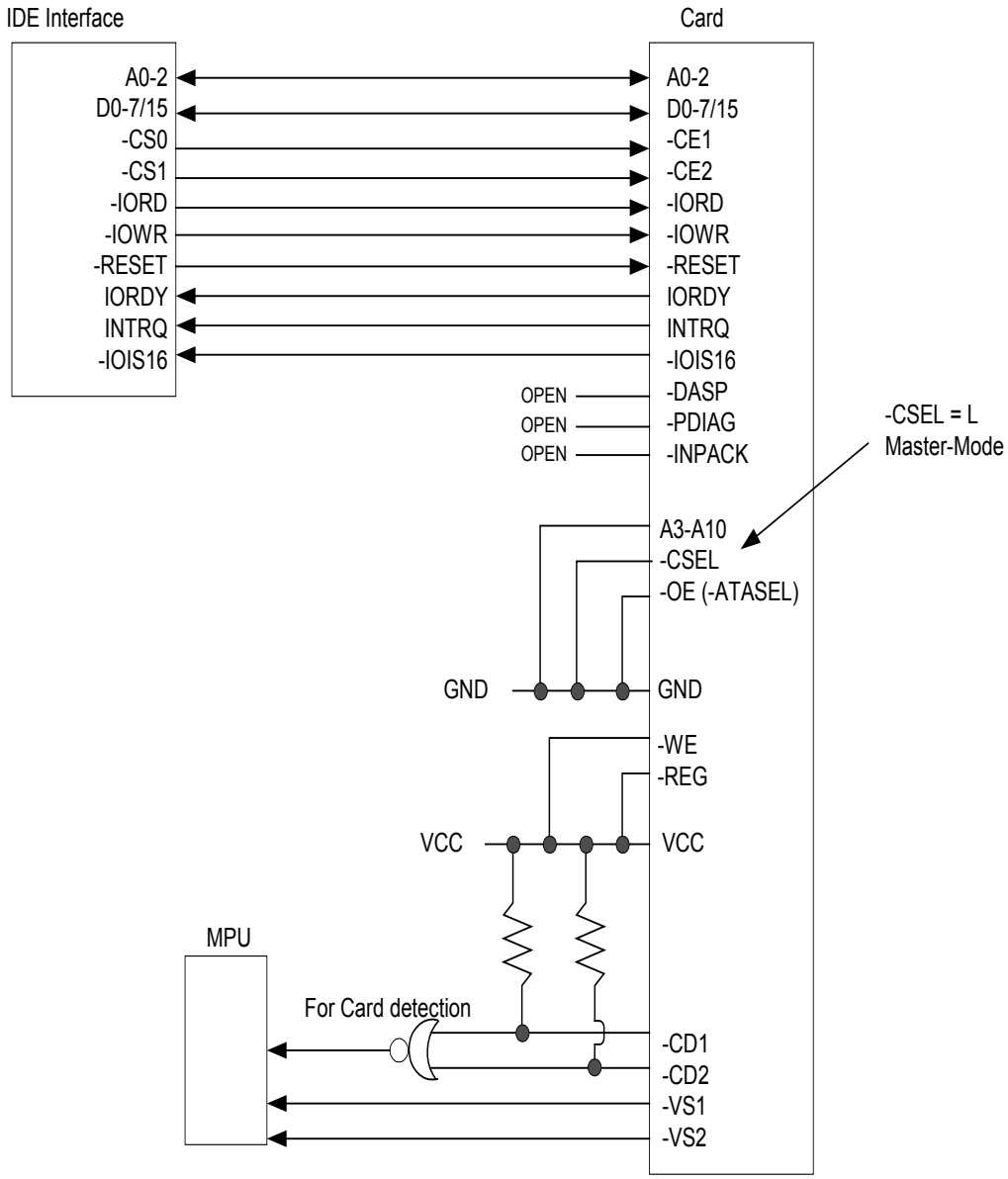
ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPERAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Figure 30: True IDE Mode I/O Timing Diagram

A. Pin Connection in True-IDE Mode

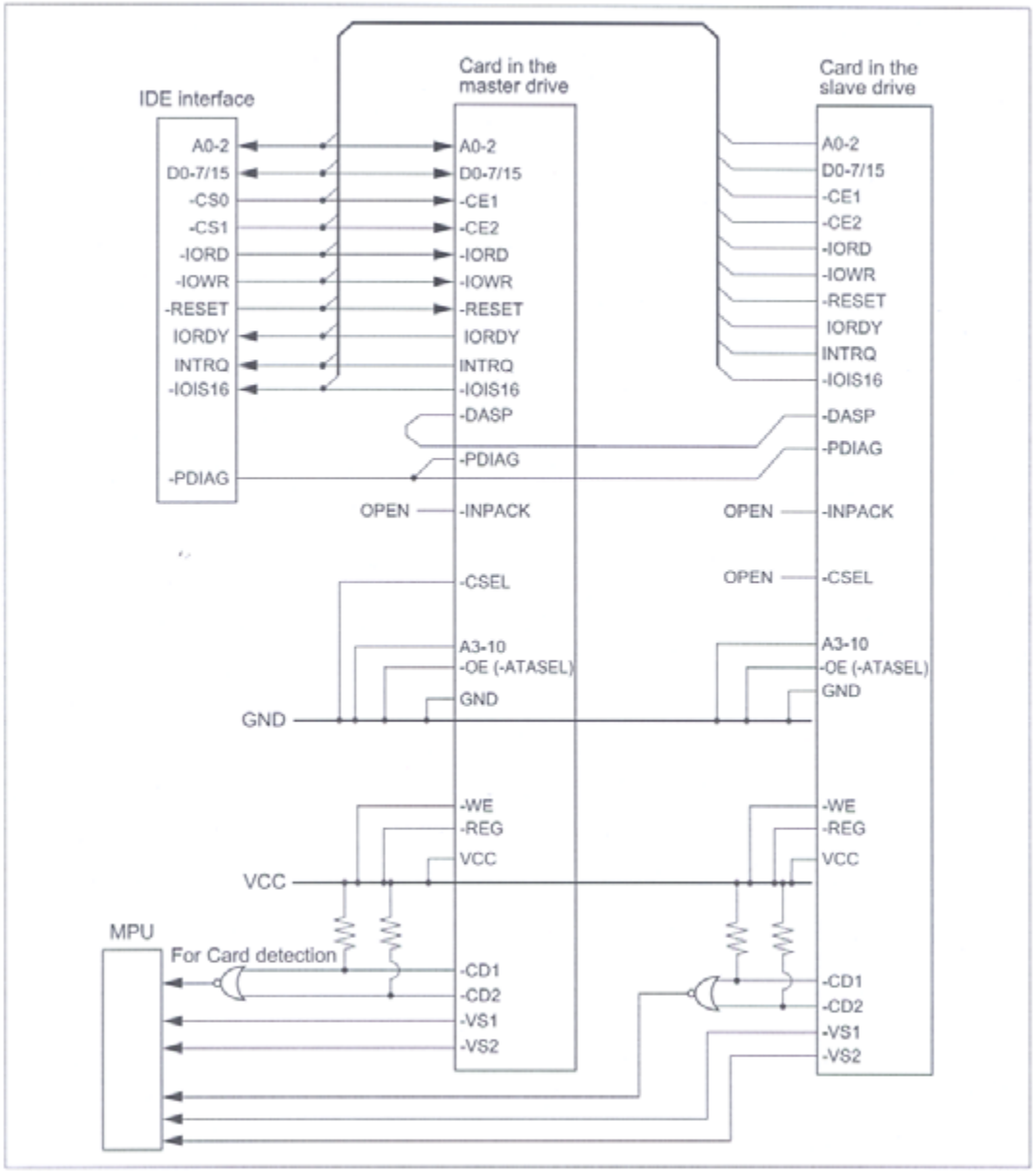
There are two ways of using cards in the True-IDE mode, namely, using only one card as the master drive and using two cards as the master and slave drives. Pin connection in each method is described below.

(1) Pin connection when only one card is used as the master drive. (example)



Note: In this case slave drive should not be accessed.

(2) Pin connection when two cards are used as the master and slave drives. (example)



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